

DRSSTC BUILDING THE MODERN DAY TESLA COIL

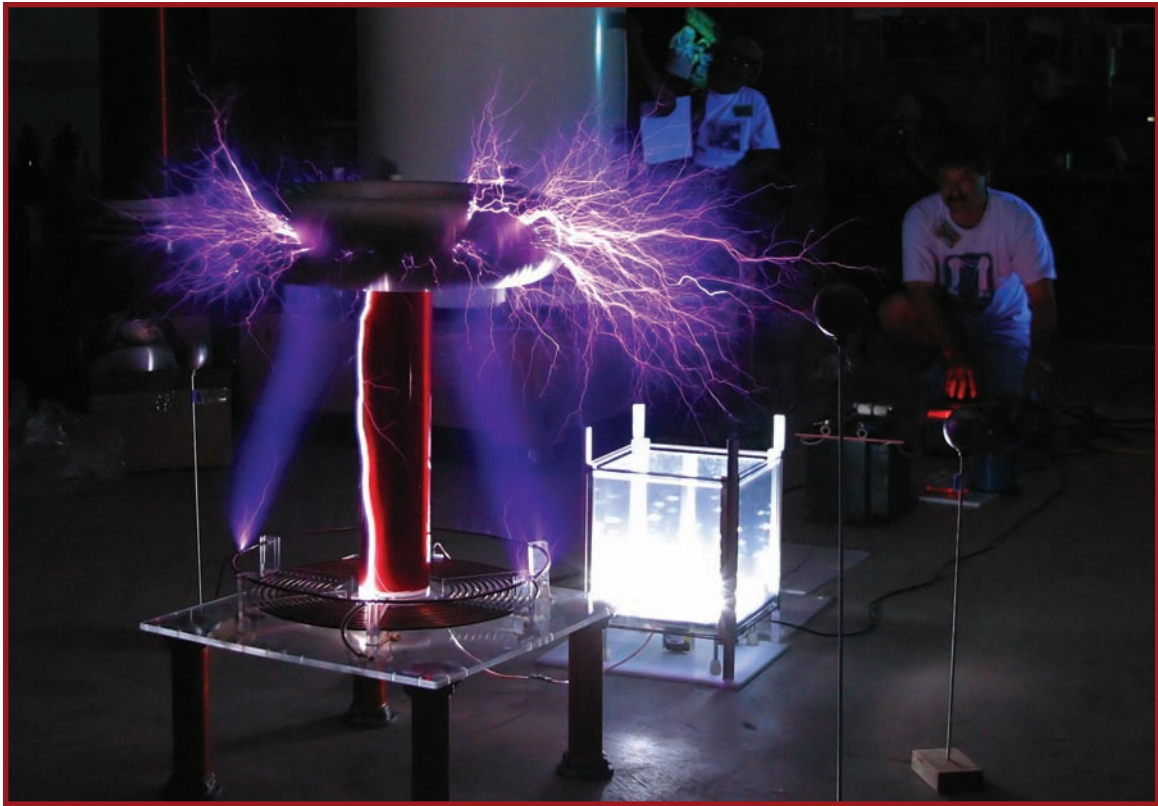
FIRST EDITION

Daniel H. McCauley IV

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Terry Blake's 14.4kV potential transformer powered Tesla coil at the 2004 RATCB

About 100 years ago, Nikola Tesla invented the first Tesla coil. Since that time, amateur scientists and students from around the world have been duplicating and improving on his first experiments in the quest for larger and more spectacular arcs. And although there were many advancements and improvements made to the Tesla coil during the 20th Century, the basic design has remained practically identical to that first used by Tesla in the late 1800's. This basic design, which is often referred to as a “conventional” or “disruptive” spark gap Tesla coil is made up of the following components:

- High voltage transformer
- Primary capacitor
- Mechanical spark gap switch
- Primary coil
- Secondary coil
- Topload

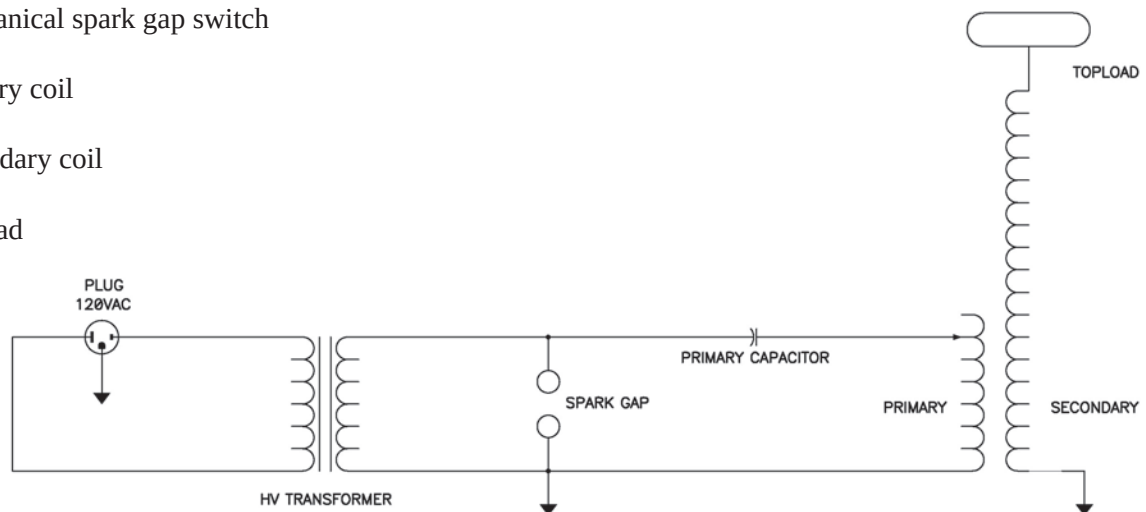


Figure 1-1 *Conventional Disruptive Spark Gap Tesla Coil*



DRSSTC System Components (First Generation)

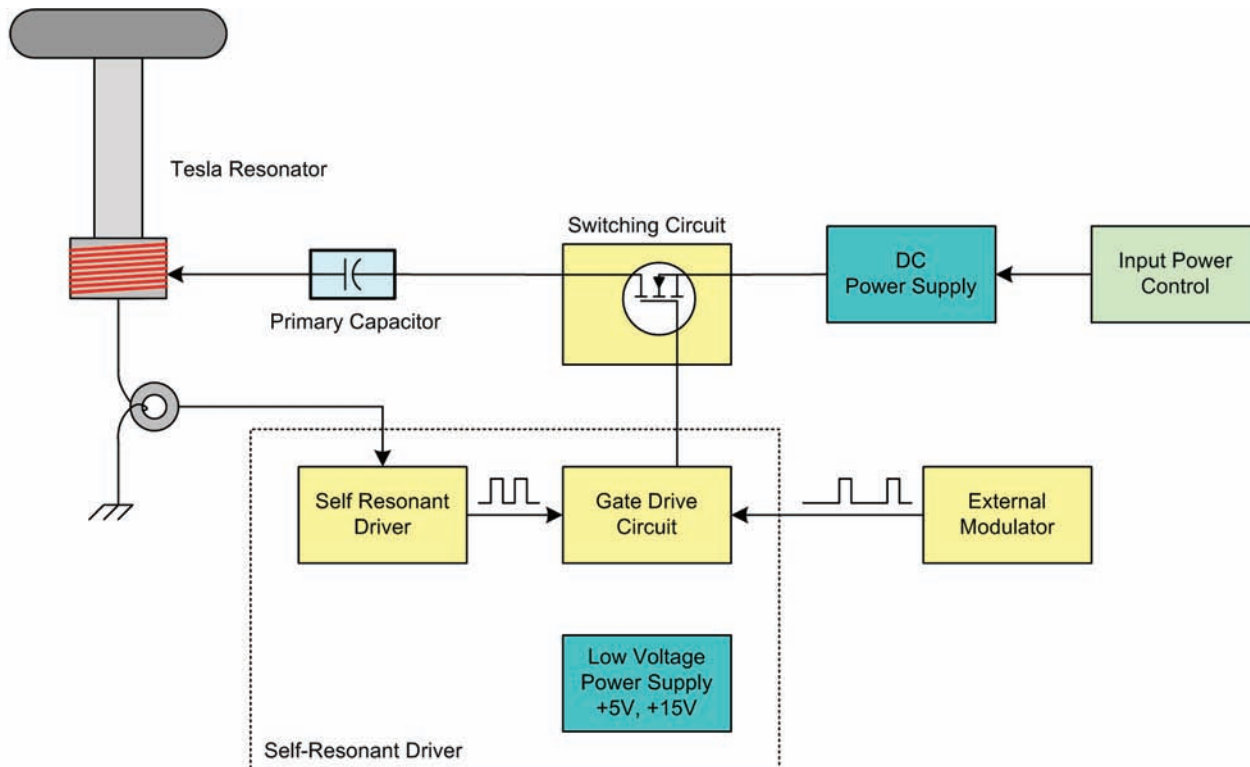


Figure 2-1 First Generation DRSSTC Block Diagram

A typical First Generation DRSSTC is made up of the following components as shown above in Figure 2-1.

- Input Power Control (Variac)
- DC Power Supply
- Self-Resonant Driver
- Full-Bridge Switching Circuit
- Tesla Resonator (Primary and Secondary Coils, Toroid)
- External Modulator

Input Power Control

The input power control to the DRSSTC system is a component which allows one to vary the input voltage to the DC power supply. For most cases, this is simply a variable transformer, or variac, that allows 120VAC or 240VAC to be continuously adjustable from 0-140VAC or 0-280VAC respectively.

DC Power Supply

A DC Power Supply is used to provide the input voltage to the full-bridge switching circuit. This can be as simple as a bridge rectifier circuit, as is used with the DRSSTC systems presented in this text, or a switching power supply. For the DRSSTCs presented in this book, a bridge rectifier circuit is used to convert 0-280VAC into 0-395VDC.

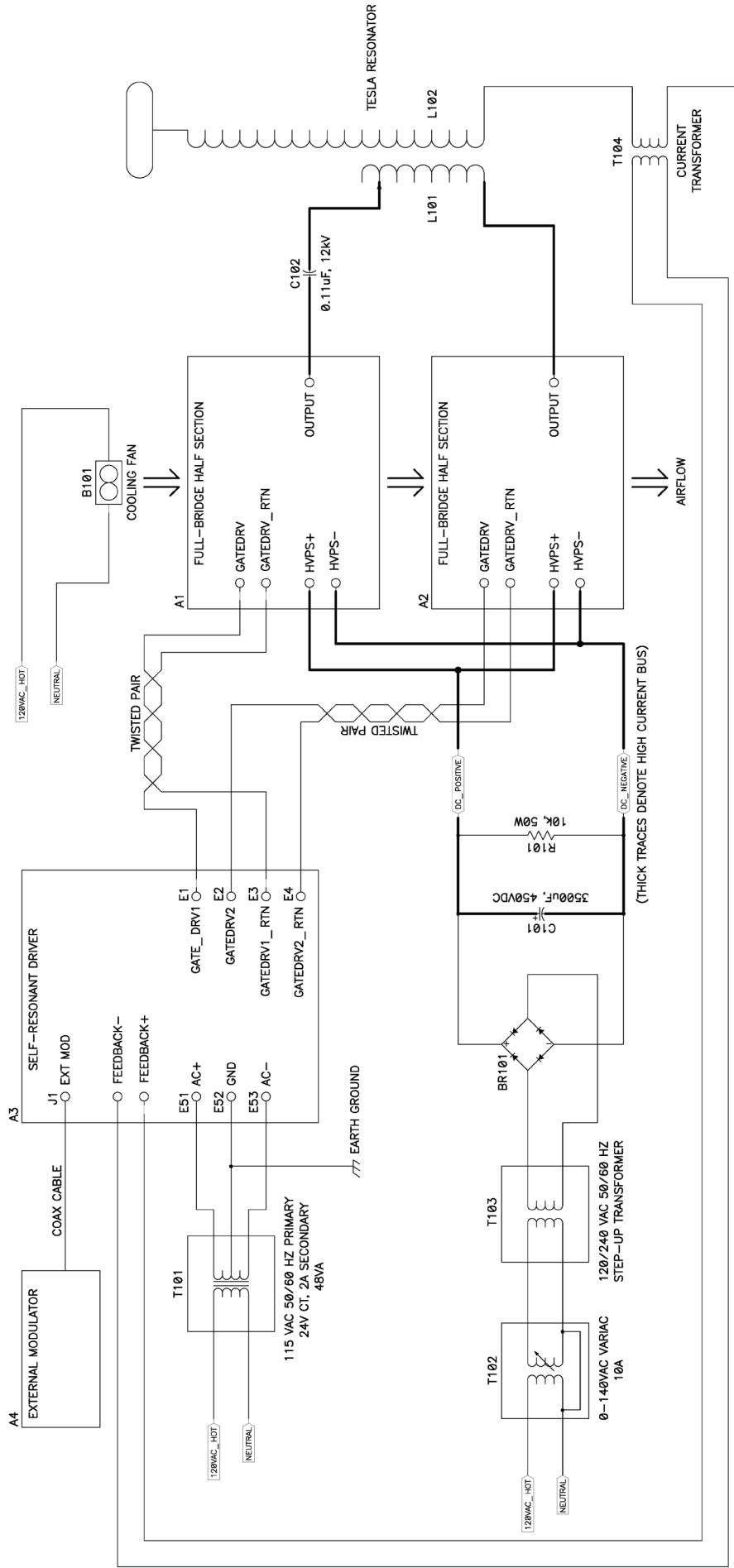


Figure 3-3 DRSSTC II Top Level System Schematic

Notes:

1. Gate drive connections between A3 and A1, A2 should be as short as possible and twisted for minimal inductance.
2. Thick traces denote high current bus connections.

Item	Ref Des	Part No.	Description	Distributor	Qty
1	A4		External Modulator Assembly	N/A	1
2	A3		Self-Resonant Driver Assembly	N/A	1
3	A1, A2		Full-Bridge Half Section Assembly	N/A	2
4			Tesla Resonator	N/A	1
5	BR101	26MB100A	Bridge Rectifier, 1000V, 25A	Allied Electric	1
6	C101	9629L95	3500uF, 450VDC Electrolytic Capacitor	Allied Electric	1
7	C102		Primary Capacitor (MMC) Assembly	N/A	1
8	R101	RH-50 10K00	Resistor, 10k, 50W	Newark	1
9	T101	166L24	Filament Transformer, 115VAC 50/60Hz Pri, 24VAC CT Sec, 48VA	Allied Electric	1
10	T102		Variable Transformer, Variac, 0-140VAC, 10A	See note 1	1
11	T103		120/240VAC 50/60Hz Step-Up Transformer	See note 1	1
12	T104		Secondary Base Current Transformer, 70:1 Ratio	N/A	1
13	B101	MX2A3	Fan, 120VAC, Comair-Rottron	Allied Electric	1

Table 3-1 *Top Level Assembly Parts List*

Notes:

1. The least expensive place to procure these items are from internet auction websites and surplus suppliers.
2. The value of C101 is not critical. Any value between 3000uF and 5000uF, rated for at least 400VDC, should work.
3. The bleed resistor, R101, is presently sized to discharge a 3500uF capacitor charged to 340VDC to less than 30V in approximately 2 minutes. If faster discharge times are required, a low resistance shorting switch should be used.

Full-Bridge Power Assembly

The full-bridge power assembly provides the high frequency, high current power necessary to drive the primary coil of the DRSSTC. For this particular system, the full-bridge power assembly is comprised of two half-section boards and is mounted on an extruded aluminum heatsink which is air cooled via a 120VAC muffin fan. Each half-section board represents one half of the full-bridge and uses two high current IGBTs which are bolted directly to the heatsink underneath. Because the gates of the IGBTs are floating at a potential above ground and swinging with respect to the positive and negative DC supply rails, high voltage insulated gate transformers are required to drive them properly. Each gate transformer has a single primary winding and two secondary windings - one secondary winding for each IGBT on the half-section board. The gate transformers receive $\pm 15\text{V}$ from the self-resonant driver board and output $\pm 30\text{V}$ to the gates of each respective IGBT. There are also numerous transient voltage suppressors (TVS) used on the board which help to suppress high voltage spikes that might occur during operation which could damage the IGBTs. Transient voltage suppressors (TVS) are used on both the input side (gate-emitter) and the output side (collector-emitter) of the IGBTs.

Full-Bridge Top Assembly

The full-bridge power assembly shown in Figure 3-1, shows how the full-bridge interfaces to the DC power supply via a high current bus bar. Because there are peak currents of over 500A within the primary circuit, custom built bus bar connections made using Kapton insulated copper was used. This bus bar connects the full-bridge power assembly to the DC power supply. Also, there are two 4.7 μF , 600V polypropylene capacitors which are placed across the DC power supply rail which are used as RF bypass capacitors. These capacitors are shown in Figure 3-4 below.

Also, it is important to note that the bus bar arrangement used in the DRSSTC II system is not optimal. In Figure 3-1, you can see that there is a large loop area created by the bus bar which creates a large amount of inductance. This inductance in turn creates large magnetic fields which induce noise onto sensitive circuitry. However, for this particular system, I have not found the added inductance to affect performance or operation in any way. But, if you plan to build your own DRSSTC, and wish to create your own custom bus bar, I would recommend designing one that minimizes the loop area thereby reducing inductance and the generation of magnetic fields.

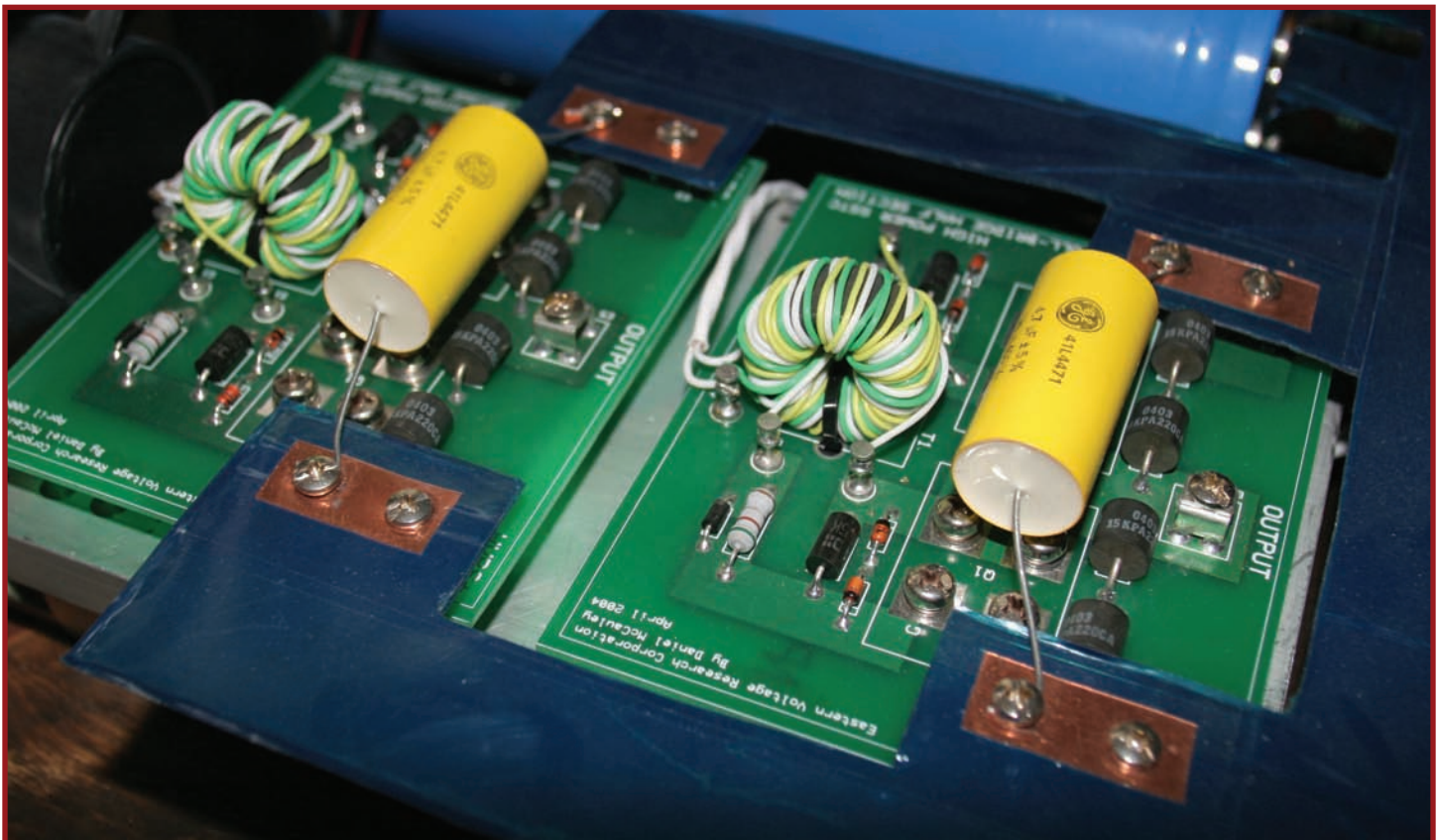


Figure 3-4 Full-Bridge Power Assembly and RF Bypass Capacitors

External Modulator

The external modulator is used to allow the operator to adjust the operation of the DRSSTC system from a safe distance. It connects directly with the self-resonant driver board via a shielded coaxial cable and allows the user to vary both the pulsewidth and pulse repetition frequency (PRF) of the system through the use of two single turn potentiometers.

Operational Specifications:

- Pulsewidth - Adjustable from 58us to 285us
- Duty Cycle - Adjustable from 0.3% to 8.6%
- Pulse repetition frequency (PRF) - Adjustable from 60Hz to 300Hz

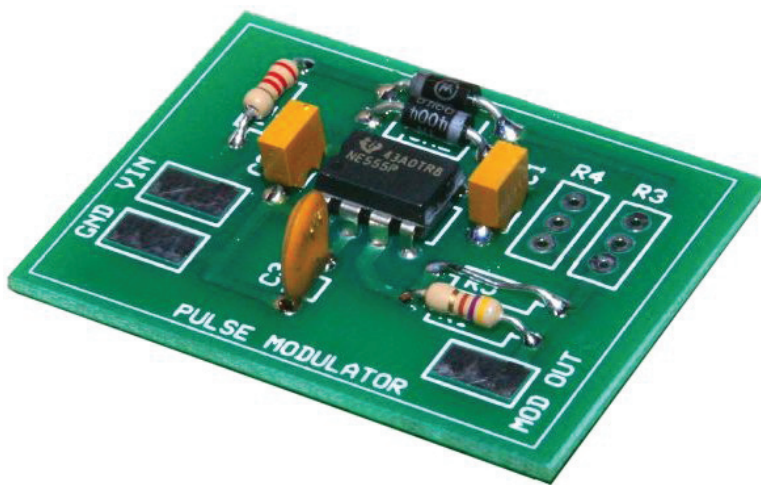


Figure 3-15 External Modulator Board and Finished Assembly

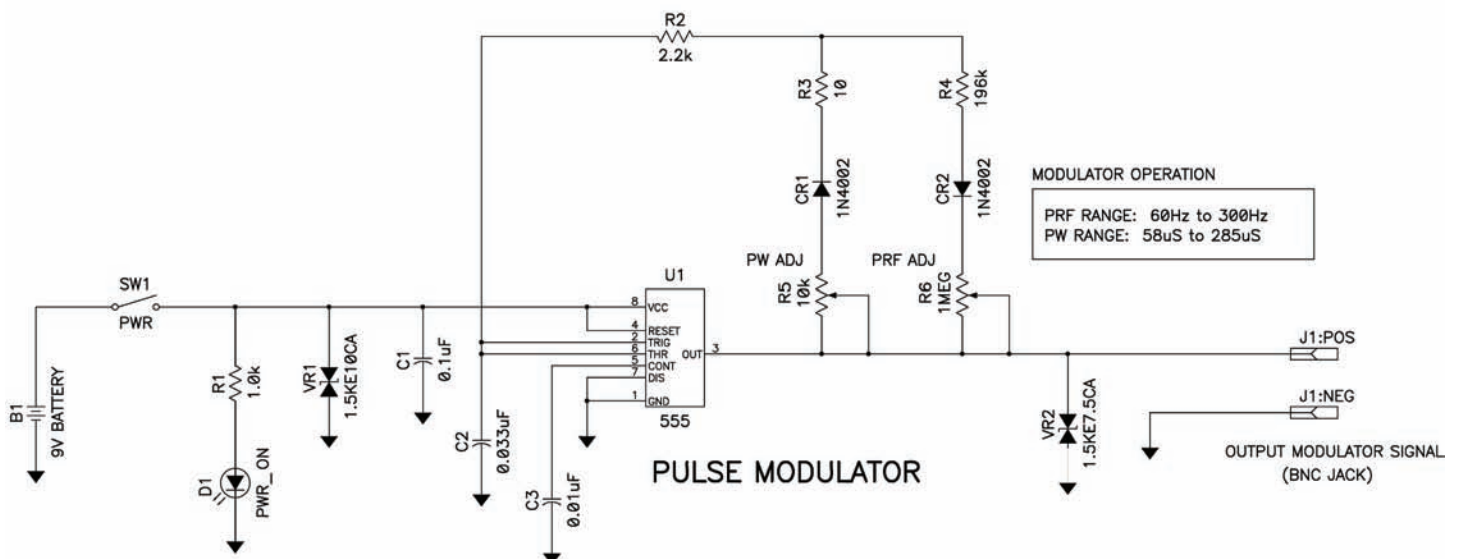


Figure 3-16 External Modulator Schematic

Top Mounting Plate Detail

The following is the detail drawing of the coil base top mounting plate as viewed from the top.

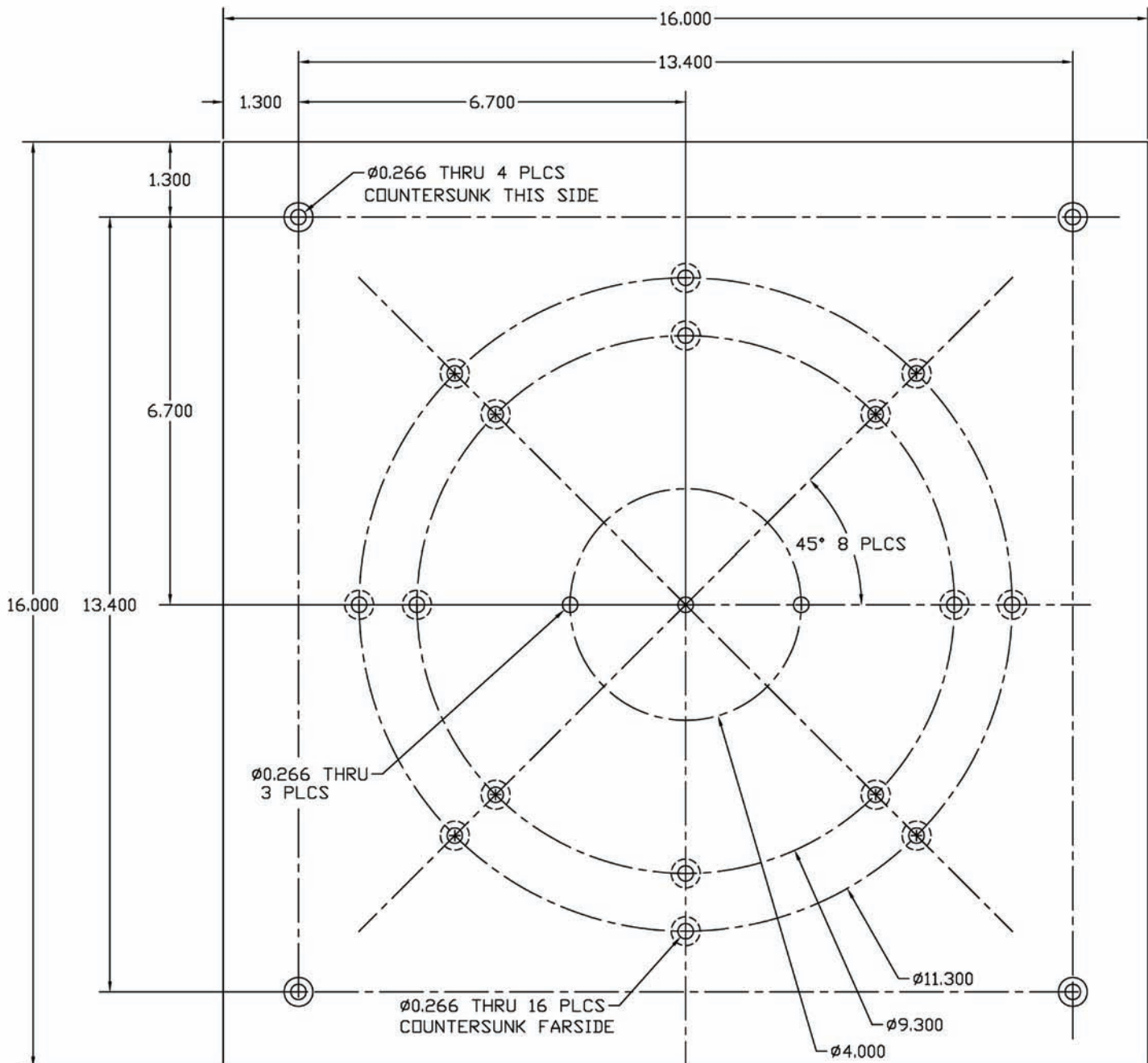


Figure 4-2 Top Mounting Plate Detail (Top View)

Notes:

1. Use a router with a standard round-over bit as necessary to round the topside edges of the mounting plate.
2. Stain and finish the mounting plate as desired.

Material Specification

16" x 16" x 3/4" Poplar (or similar)

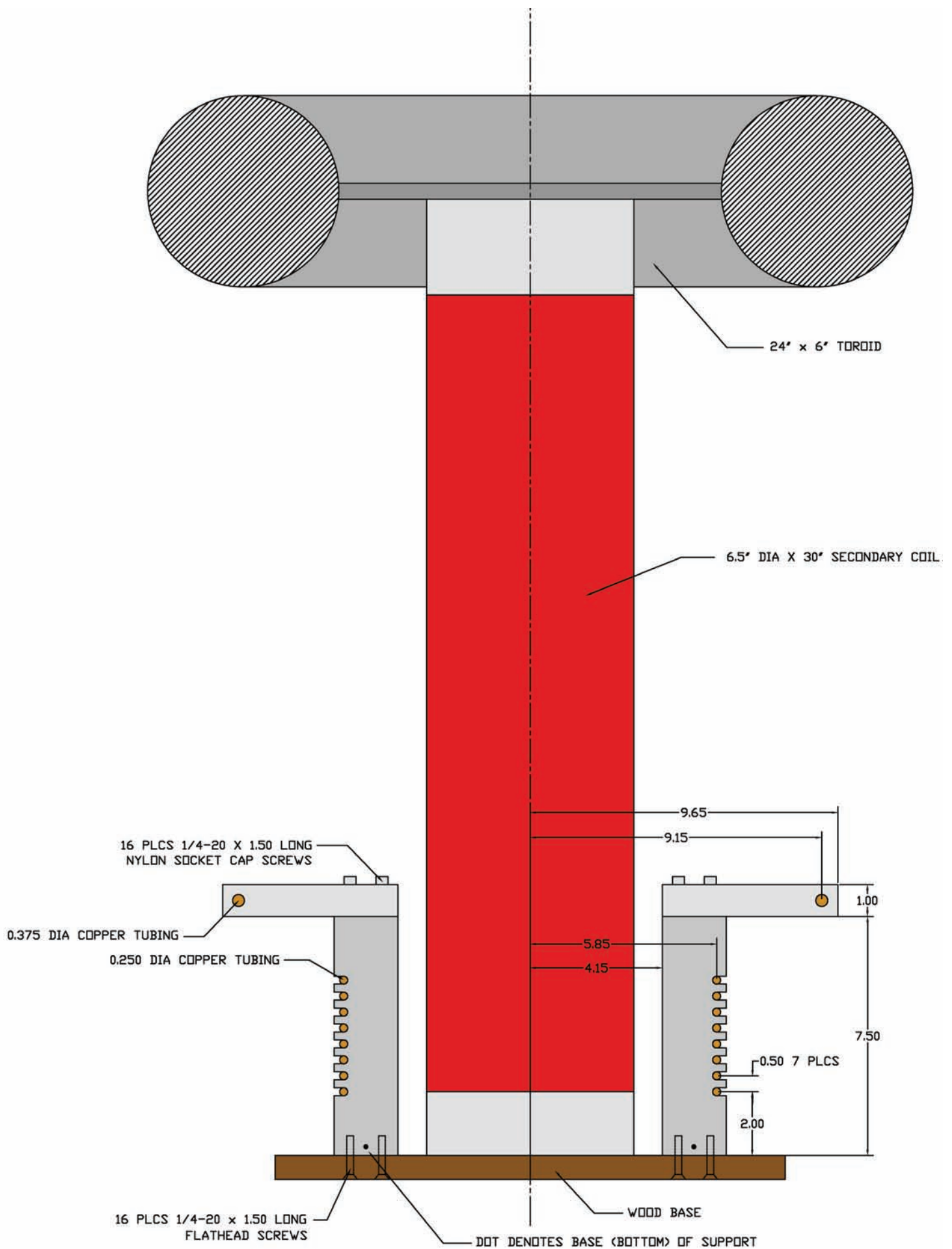


Figure 4-11 *Assembly Dimensional Detail (Side View)*



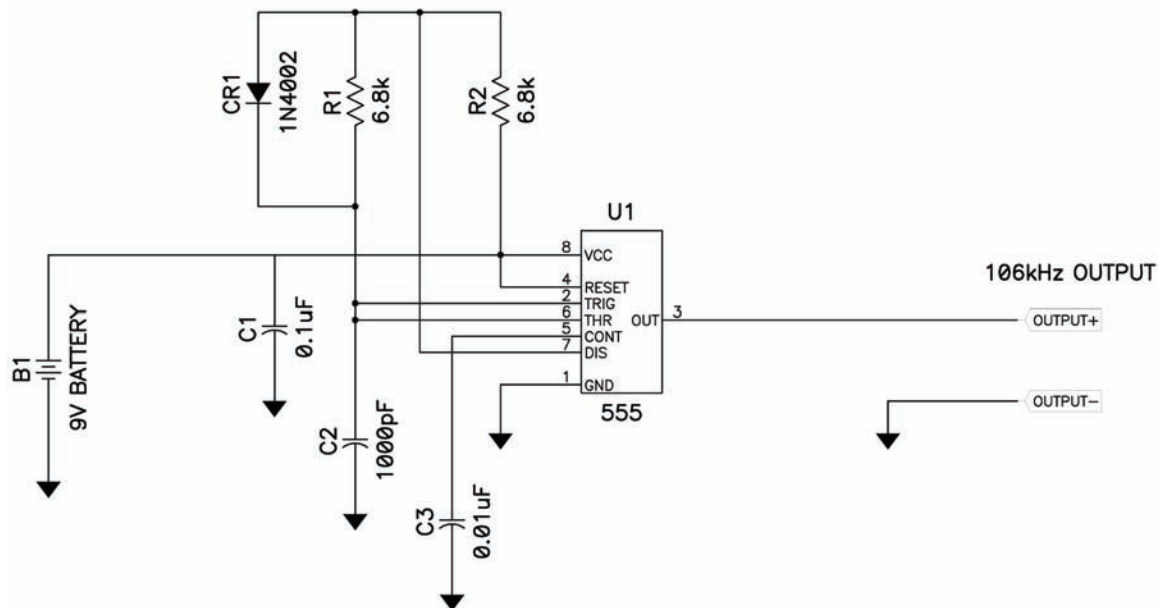


Figure 5-1 100kHz Square Wave Generator Schematic (106kHz actual)

10. Apply power to the self-resonant driver board and enable the signal generator.
11. Using an oscilloscope, verify that the following signal shown in Figure 5-2 is present on pin 2 of U2-U6.

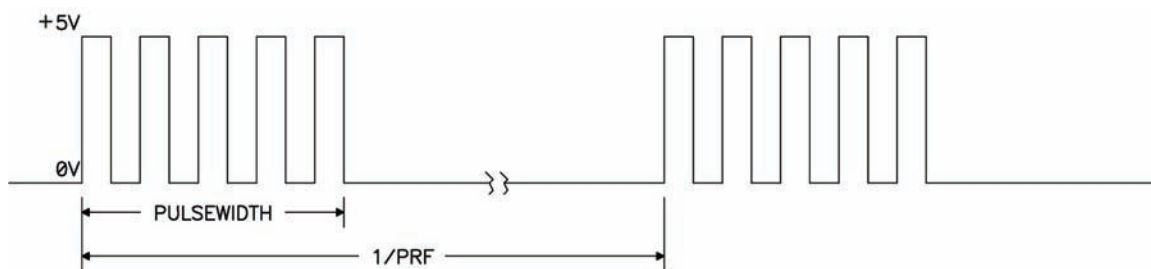


Figure 5-2 Gate Driver IC Input Waveform

12. Remove power from the self-resonant driver board, disable the signal generator, and install components U2-U6.
13. Apply power to the self-resonant driver board, enable the signal generator, and using an oscilloscope verify that the following signals shown in Figure 5-3 are present across the output terminals E1 to E3, and E2 to E4. These signals are not ground referenced, so a differential measurement, using oscilloscope two probes, must be taken with the oscilloscope.

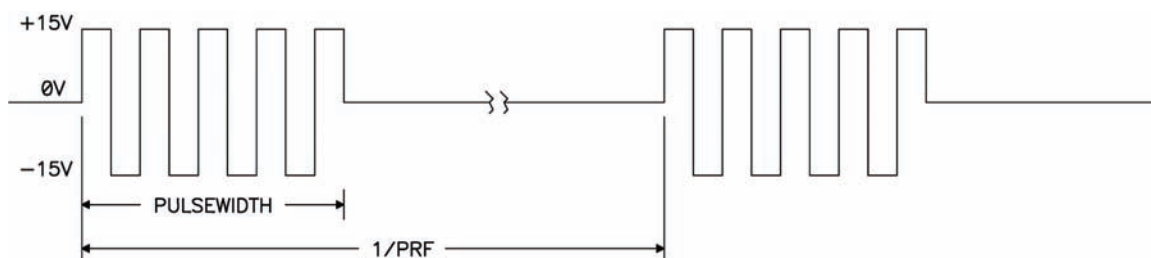


Figure 5-3 Gate Driver IC Output Waveform (Push-Pull Configuration)

2. Connect the test circuit as shown below in Figure 5-8. An HP 200CD oscillator is recommended due to its high power output capabilities, but a standard signal generator will work as well.

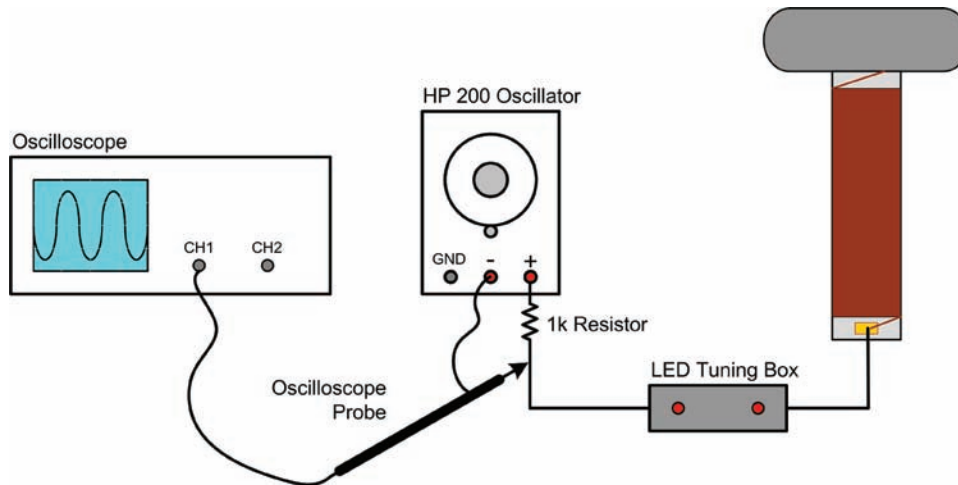


Figure 5-8 *Secondary Coil Resonant Frequency Measurement Set-up*

3. To begin the test, set the signal generator for maximum output amplitude and initially set the output frequency to the estimated resonant frequency of the secondary coil assembly. Manually sweep the output frequency of the signal generator to determine the resonant frequency of the secondary coil assembly. Series resonance is defined as the point where the series LC circuit is at minimum impedance, therefore the resonant frequency will be the point where the LED indicator is at its brightest and the amplitude shown on the oscilloscope is at its maximum.

4. Once the resonant frequency of the secondary coil assembly is determined, the next step is to determine the initial tuning point of the primary coil. Connect the test circuit as shown below in Figure 5-9. Set the signal generator for maximum output amplitude, and set the output frequency of the signal generator to the measured secondary coil resonant frequency which was determined in step 3 above. Verify the output frequency of the signal generator using the oscilloscope to ensure accuracy.

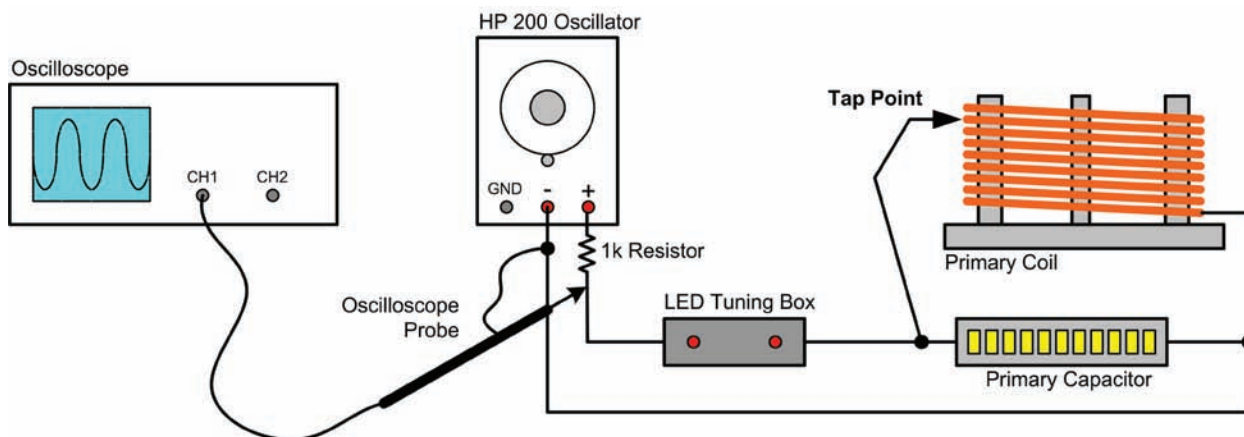


Figure 5-9 *Primary Coil Initial Tuning Set-up*

5. In this step, you will begin moving the upper tap of the primary coil until the point of resonance is found. Parallel resonance is defined as the point where the parallel LC circuit is at maximum impedance, therefore, the point of resonance will be where the LED indicator is at its dimmest, and the amplitude shown on the oscilloscope is at its minimum.

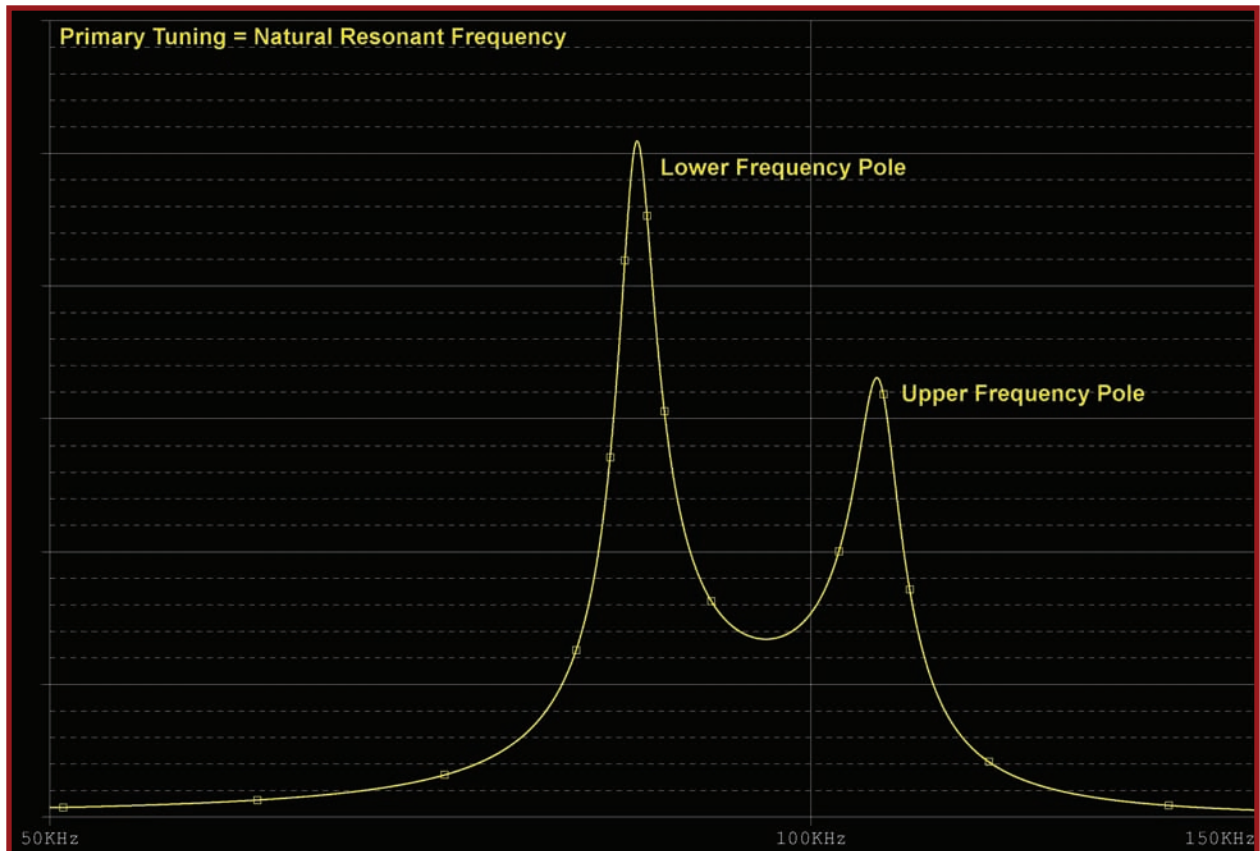


Figure 5-11 *Frequency Splitting in a Tesla Resonator*

It should be understood that when frequency splitting occurs, energy will tend to transfer back and forth between primary and secondary circuits and create notches at the frequency equal to the difference in frequencies between upper and lower poles. The frequency at which the notches occur is commonly known as the beating frequency. With relatively lower power DRSSTC systems (less than 2kW) such as the Second Generation DRSSTC systems presented in this text, notching in the primary current, as shown in Figure 5-12 below, will limit the amount of energy transfer in the primary circuit and reduce the overall bang energy of the system. To solve this, we merely need to detune the primary circuit to a frequency lower or higher than the natural resonant frequency of the uncoupled secondary circuit. When the primary circuit is detuned lower than the natural

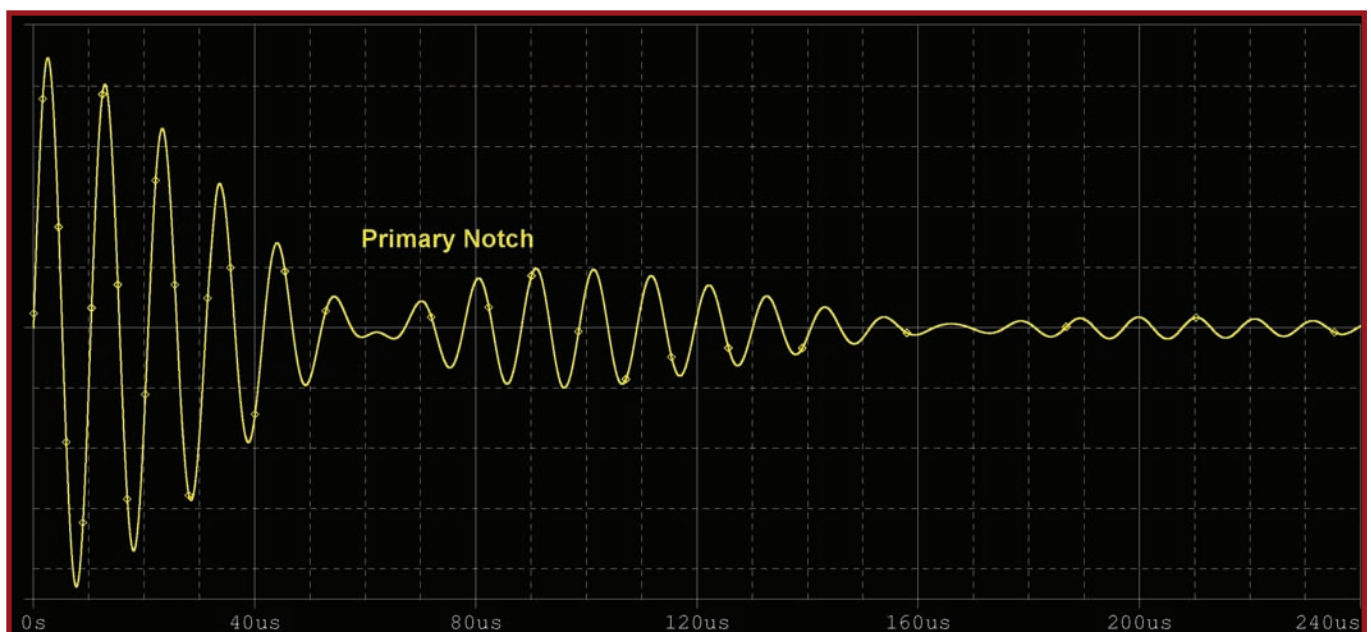


Figure 5-12 *Primary Current Notching*

Secondary Base Current Transformer PSpice Simulation

The PSpice simulation circuit shown below in Figure 6-2 was used to evaluate the performance and aid in the design of the current transformer which is used to sample the secondary base current. This sampled current is then used as positive feedback to derive the gate signals to drive the full-bridge switching circuit.

Secondary Base Current Transformer PSpice Model

The PSpice circuit used to model the secondary base current transformer shown below in Figure 6-2 is comprised of several key components. Isecondary is a sinusoidal current source used to model the secondary base current. Its frequency is set at 100kHz which is the resonant frequency of the DRSSTC II system. The current transformer is created using the PSpice K_Linear model where inductances of each winding and the coupling between them is used to define the transformer. Cdecoupling is used to prevent any DC bias from flowing back into the current transformer and Rlimit is used to limit the current flowing into the 7414 schmidt-trigger inverter IC. Diodes, D1 and D2, are used to clamp the output voltage of the current transformer to between 0V and 5V. The logic level output of the 7414 schmidt-trigger inverter IC, which is used to drive the gate driver ICs in the actual system, is labeled as “drive.”

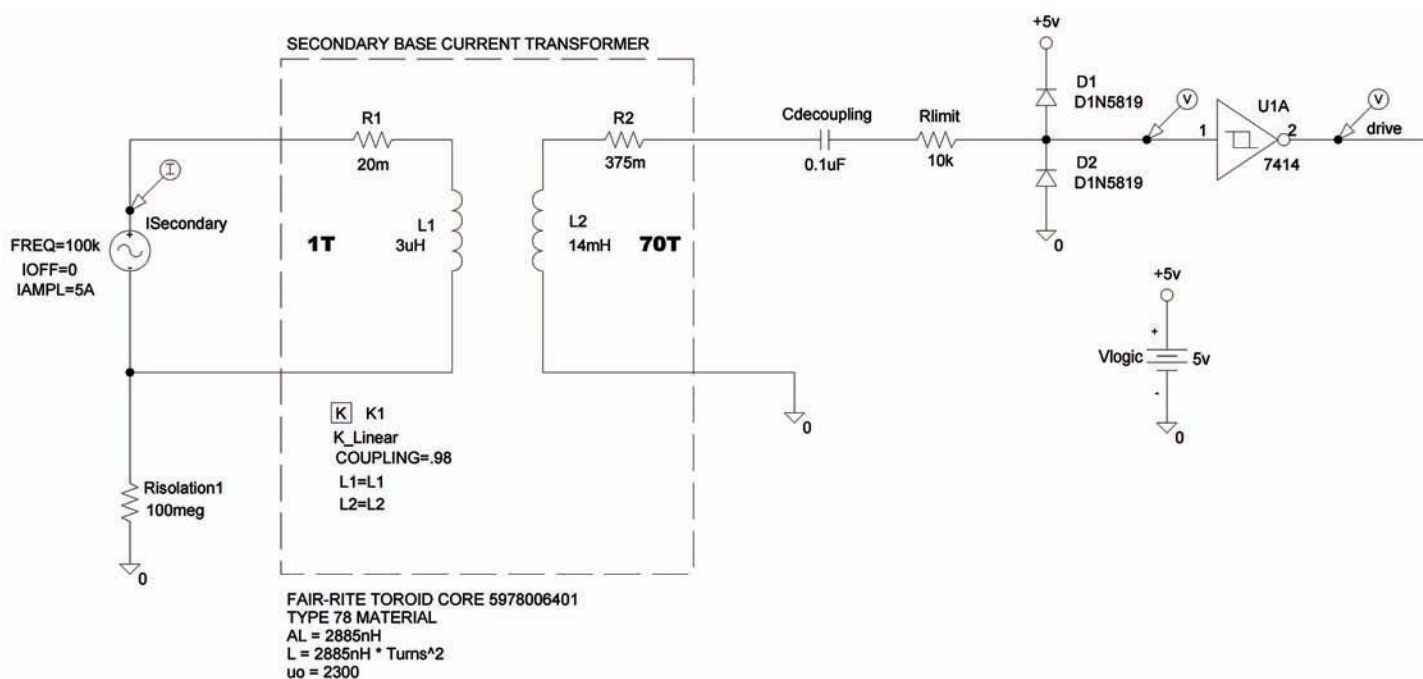


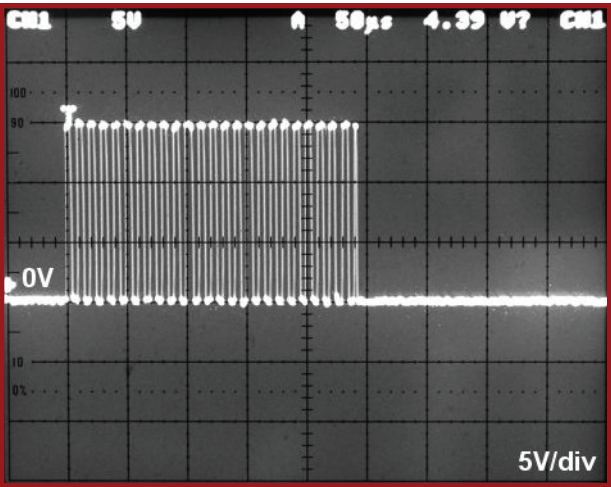
Figure 6-2 PSpice Secondary Base Current Transformer Model

Secondary Base Current Transformer PSpice Results

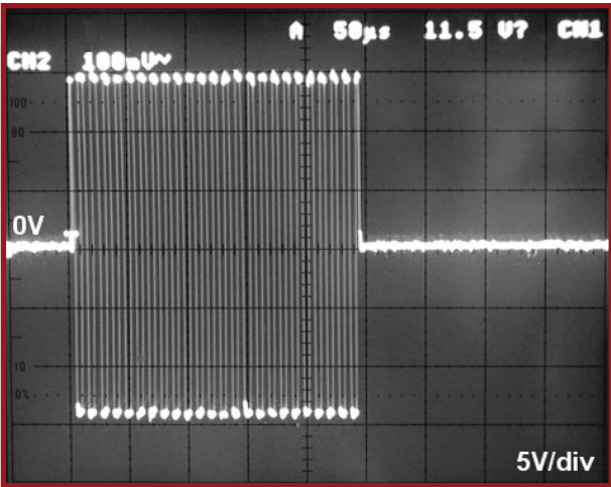
The PSpice model was simulated for varying magnitudes of secondary base current ranging from 10mA to 10A. The waveforms shown on the facing page show the results for two iterations where the secondary base current was set to 1A and 5A. There are three waveforms displayed per plot which are designated as follows: The yellow waveform shows secondary base current, the blue waveform shows the voltage level at the input to the 7414 schmidt-trigger inverter IC, and the white waveform shows the logic level output drive signal which is the final output for this PSpice circuit.

In each instance, the circuit works as expected. There is a slight phase shift between the secondary base current and the final logic level output drive, but given the nature of the circuit, this was expected.

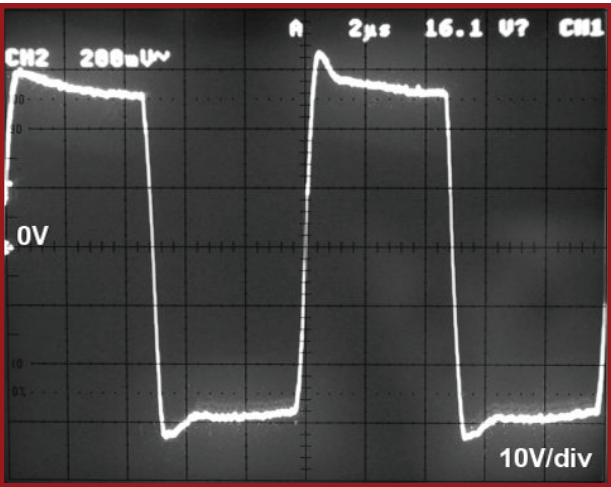
IGBT Gate Driver Waveforms



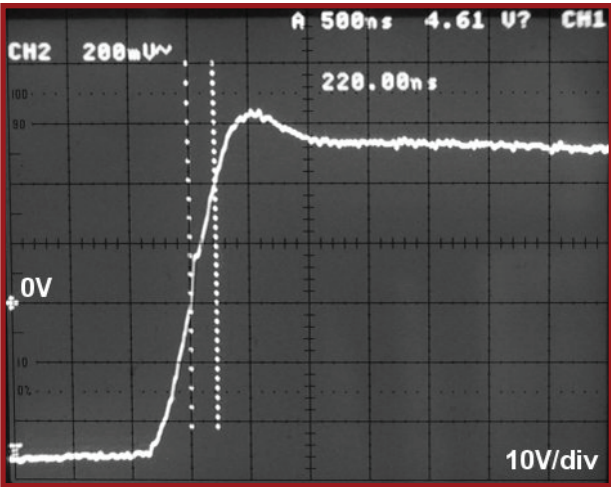
Single Pulse Burst (250us)
Output of UCC37322 Gate Driver IC



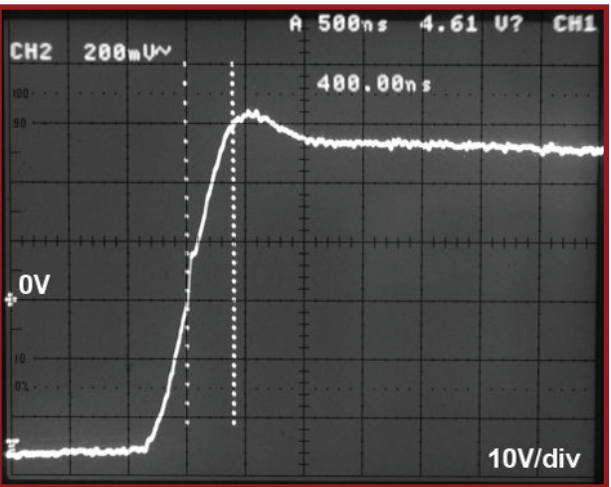
Single Pulse Burst (250us)
Output of Self-Resonant Driver Board (E1 to E3)



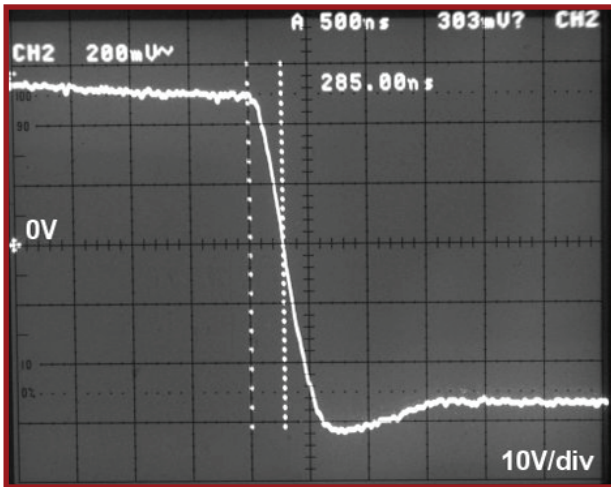
V_{GE}
Measured at IGBT Gate (100kHz)



V_{GE} Risetime
220ns (0V to 20V)



V_{GE} Risetime
400ns (0V to 30V)



V_{GE} Falltime
285ns (25V to 0V)



Above

Photographer Terry Blake managed to capture this awesome exposition of the DRSSTC II system during its first demonstration at the 2004 Rochester Area Tesla Builders (RATCB) Teslathon at Ed Wingate's high voltage lab. Arcing from primary to secondary is evident in this photo and most likely led to the failure.

Right

Ribbons of arc dance across the air in this close-up image of the DRSSTC II striking a nearby mirror. Each individual arc channel occurs every 10ms and both air current and heat cause the undulating nature of the arc channels as shown here.

Primary Current Feedback PSPICE Simulation

The PSPICE simulation circuit shown below in Figure 10-6 was used to evaluate the performance and to aid in the design of the primary current feedback circuit which is used to sample the output current of the full-bridge switching circuit and use it to derive the gate drive for the system. Unlike a First Generation design which samples low current, on the order of 5-10A maximum, the current transformer in a Second Generation design must be able to sample current in the primary circuit on the order of several hundred amps. Under normal operating conditions, the DRSSTC II system produces approximately 500A peak current in the primary circuit and during ground strikes, primary current can exceed 800A!

Primary Current Feedback PSPICE Model

The PSPICE model used to model the primary current feedback circuit shown below in Figure 10-6 is comprised of several key components. Instead of using a current source for this model, a voltage source, Vprimary, was used in conjunction with a series output load resistance, Rsource, to create the necessary current in the primary winding. For this example, primary current is approximately equal to $V_{\text{primary}} / (R_{\text{source}} + R_1)$. The frequency of Vprimary is set at 100kHz which is the resonant frequency of the DRSSTC II system. For this Second Generation design, a commercial-off-the-shelf high frequency current transformer was used and the parameters from its datasheet were used to create the primary feedback current transformer model as shown. The most important parameters used are the winding inductances, and the output DC series resistance, which for this transformer is 0.580 ohms. As was done previously, the current transformer was created using the PSPICE K_Linear model where inductances of each winding and the coupling between them is used to define the transformer. Since the current transformer is loosely coupled, I estimated the coupling coefficient between windings as 0.98. Diodes, D2 and D3, are 4.7V zener diodes used to clamp the output voltage of the current transformer to between +4.7V and -4.7V and Schottky diodes, D1, and D4, are used to “block” the slow recovery of the zener diodes. Cdecoupling is used to prevent any DC bias from flowing back into the current transformer and Rlimit is used to limit the current flowing into the 7414 schmidt-trigger inverter IC. Diodes, D5 and D6, are used to clamp the voltage at the input to the 7414 schmidt-trigger IC to between 0V and 5V. The logic level output of the 7414 schmidt-trigger inverter IC, which is used to drive the gate driver ICs in the actual system, is labeled as “drive.”

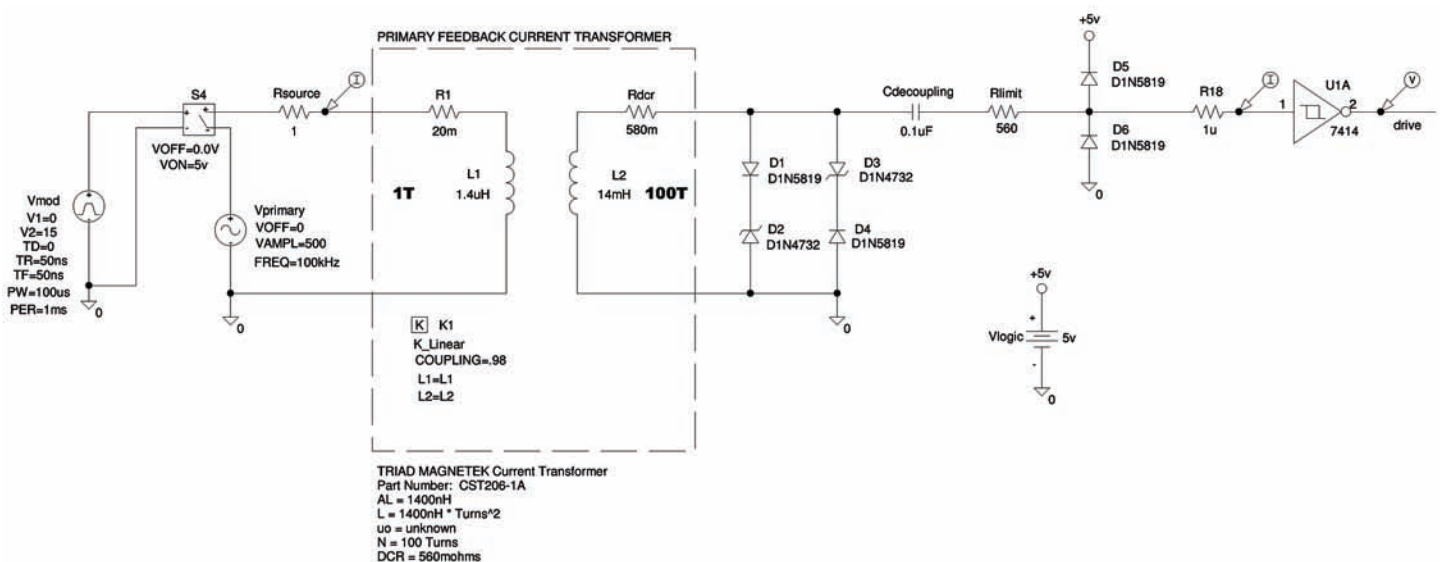


Figure 10-6 PSPICE Primary Current Feedback Model

Primary Current Feedback PSPICE Results

The PSPICE model was simulated for varying magnitudes of primary current ranging from 1A to 800A. The waveforms shown on the facing page in Figures 10-7 and 10-8, show the results for two iterations where primary current was set to 1A and 500A. There are three waveforms displayed per plot which are designated as follows: The yellow waveform shows primary current, the blue waveform shows the input current to the 7414 schmidt-trigger inverter IC, and the white waveform shows the logic level output drive signal which is the final output for this PSPICE circuit.

Rhysteresis. You'll note that there is some ripple associated with the filtered current sample waveform which is roughly centered around the reference voltage level of 3V. With the hysteresis added, the reference voltage level immediately drops to about 2V when the comparator is tripped. This prevents the ripple from re-tripping the comparator and ensures that the comparator will not trip again until the filtered current sample waveform dips below 2V. At this point, the reference voltage again resets to 3V. So in summary, the thresholds for the comparator in the PSPICE model, as shown in Figure 10-10, are listed below:

- Overcurrent threshold - 520A (Reference voltage = 3.00V)
- Comparator Reset threshold - 400A (Reference voltage = 2.00V)

One final point to note regarding the hysteresis of the comparator is that the level at which the reference voltage will drop when the comparator is tripped is dependent upon the reference voltage setpoint. Nominally, this is 1V when the reference voltage is set to 3V, however it will vary slightly as the reference voltage setpoint deviates from 3V.

The last point to discuss is the time constant of the current sample filter. Because the filtered current sample voltage is filtered through Cfilter and Rfilter, the response time of the current sample is relatively slow. For overcurrent, the response time is typically fast enough to have the comparator trip within one cycle of operation (10us @ 100kHz) which is quite sufficient for this application. The other concern is how slowly the filtered current sample waveform discharges. You'll note that in Figure 10-12, that after the first operational pulse burst, that the filtered current sample waveform takes approximately 400us to discharge to 0V. However, for the DRSSTC II system, which has a maximum pulse repetition frequency (PRF) of 330Hz and maximum pulsewidth of 300us, the minimum time needed to reset the filtered current sample voltage to 0V, in between pulse bursts, is approximately equal to 2.7ms which is more than 20 times the time constant of Rfilter and Cfilter which is 100us. So no matter what the operational pulse repetition frequency (PRF) or pulsewidth of the system, the filtered current sample waveform will always reset to 0V in between pulse bursts.

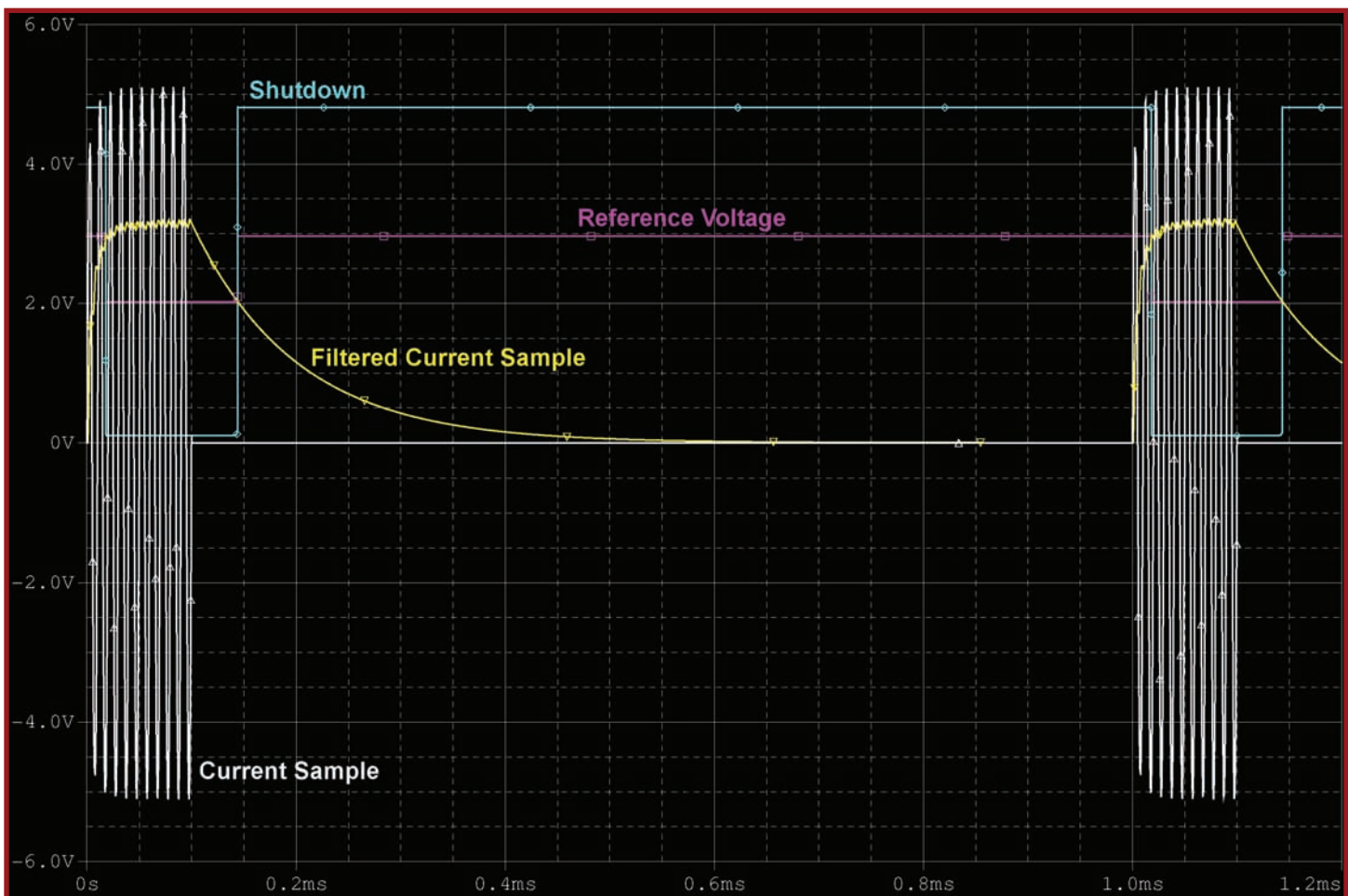


Figure 10-12 Primary Current Sample Discharge Waveforms ($I_{PRIMARY} = 525A$)